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10/583,868	06/21/2006	Tetsuya Hirano	292813US2PCT	8990
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OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
GIARDINO JR, MARK A				
ART UNIT		PAPER NUMBER		
2185				
NOTIFICATION DATE		DELIVERY MODE		
09/15/2008		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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# Office Action Summary

**Application No.**

10/583,868

**Applicant(s)**

HIRANO, TETSUYA

**Examiner**

MARK A. GIARDINO JR

**Art Unit**

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

The Examiner acknowledges the applicant's submission of the amendment dated 6/18/2008. At this point, claims 1-6 have been amended and no claims have been added. Thus, claims 1-6 are pending in the instant application.

The instant application having Application No. 10/583,868 has a total of 6 claims pending in the application, there are 4 independent claims and 2 dependent claims, all of which are ready for examination by the examiner.

**REJECTIONS BASED ON PRIOR ART**

**Claim Rejections - 35 USC ' 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kutaragi et al (US 5,111,530).

**Regarding Claim 1**, Kutaragi teaches a data processor comprising, a CPU configured to control an entire system (CPU 13 in Figure 4);

a DSP configured to perform preset processing (Signal Processor 11 in Figure 4), to have at least two bus cycles in a unit of one data access, (Figure 12E, where the DSP is taking two bus cycles to access a unit of data), and to use a selectable number

of the bus cycles in the unit of one data access; (the amount of cycles dedicated to accessing a unit of data from the memory by the DSP is adjustable as described in Column 16 Lines 28-45, note particularly how the 'access periods can be properly adjusted' on Lines 31-32) and

and an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU (External RAM 14, the host must go through the DSP to access the RAM), wherein

a data word length accessed by the DSP at the external memory is variable (time-division control circuit 94 [in Figure 10] can adjust how long the DSP accesses the memory for, Column 16 Lines 28-34); and

the DSP includes:

a determination unit configured to determine whether the DSP is accessing the external memory (the determination means corresponds to time-division control circuit 94 of Figure 10, since it determines whether the DSP or CPU is accessing the external memory, Column 16 Lines 34-45);

a control unit configured to determine whether the CPU is allowed to access the external memory, based on a signal from the determination unit (time-division control circuit 94 also acts as a control means, as it determines which device is allowed to access the memory, Column 16 Lines 34-45, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data); and

a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control unit, and to input or output the address and the data based on the switching operation (Figure 10, the latches 97-99 switch connections of the address and data signals depending on which device the time-division control circuit decides is accessing the external memory, Column 16 Lines 38-45),

wherein when the data word length is selected so that the DSP accesses the external memory using a maximum number of bus cycles, when the determination unit determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control unit (Column 16 Lines 28-58, the time-division control circuit can adjust the memory bus to be accessed the DSP only, thus the CPU is not allowed to access the memory, placing the CPU in a wait state, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data), and

when the data word length is not selected so that the DSP accesses the external memory using the maximum number of the bus cycles, the control unit is configured to allow the CPU to access the external memory by utilizing a free bus cycle (see for example, Figure 12D and Figure 12E, the last bus cycle is used by the CPU to access the external memory).

**Regarding Claim 2**, Kutaragi teaches a data processor comprising,

a CPU configured to control an entire system (CPU 13);

a sound source configured to supply a musical tone signal (ROM 1, Column 4 Lines 55-68);

a DSP configured to perform preset processing to apply a desired effect to the musical tone signal supplied from the sound source (DSP 11, also see effects processing description on Column 3 Lines 24-27), to have at least two bus cycles in a unit of one data access with respect to signal processing of the musical tone signal, (Figure 12D, where the DSP is taking two bus cycles to access a unit of data), and to use a selectable number of bus cycles in the unit of one data access (the amount of cycles dedicated to accessing a unit of data from the memory by the DSP is adjustable as described in Column 16 Lines 28-45, note particularly how the 'access periods can be properly adjusted' on Lines 31-32); and

an external memory configured to be accessed by the DSP and to be accessed through the DSP by the CPU (External RAM 14, the host must go through the DSP to access the RAM); wherein

a data word length accessed by the DSP at the external memory is variable (time-division control circuit 94 [in Figure 10] can adjust how long the DSP accesses the memory for, Column 16 Lines 28-34), and

the DSP including:

a determination unit configured to determine whether the DSP is accessing the external memory (the determination means corresponds to time-division control circuit 94 of Figure 10, since it determines whether the DSP or CPU is accessing the external memory, Column 16 Lines 34-45);

a control unit configured to determine whether the CPU is allowed to access the external memory, based on a signal from the determination unit (time-division control circuit 94 also acts as a control means, as it determines which device is allowed to access the memory, Column 16 Lines 34-45, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data); and

a switching unit configured to perform a switching operation of an address and a data in connection with the external memory according to a command from the control means, and to input and to output the address and the data based on the switching operation (Figure 10, the latches 97-99 switch connections of the address and data signals depending on which device the time-division control circuit decides is accessing the external memory, Column 16 Lines 38-45),

wherein when the data word length is selected that the DSP accesses the external memory using a maximum number of bus cycles, when the determination unit determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control unit (Column 16 Lines 28-58, the time-division control circuit can adjust the memory bus to be accessed the DSP only, thus the CPU is not allowed to access the memory, placing the CPU in a wait state, also see Column 3 Lines 60-65, where the CPU [control means of lines 62-63] is only allowed to access data when the processing means is not accessing data), and

when the data length is not selected that the DSP accesses the external memory using the maximum number of the bus cycles, the control unit is configured to allow the

CPU to access the external memory by utilizing a free bus cycle (see for example, Figure 12D and Figure 12E, the last bus cycle is used by the CPU to access the external memory).

**Claim Rejections - 35 USC ' 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kutaragi in view of Davis et al (US 4,991,169).

**Regarding Claim 5**, Kutaragi teaches a data processor having a fixed number of memory access timings per sampling cycle (Column 16 Lines 8-11, one sampling cycle [corresponding to a machine cycle in Kutaragi] has a fixed number of memory accesses allowed, based on the timing RAM access times and length of the machine cycle) and an external memory storing musical tone waveform data (ROM 1, Column 4 Lines 55-68);

the data processor comprising:

a first selector configured to output an address from the allowed DSP in response to a determination signal from the access determination unit (switch 97 in Figure 10, note how this outputs an address from the DSP to the external memory);

However, Kutaragi does not teach multiple DSPs with a shared RAM. Davis teaches a plurality of DSPs (DSP 20 and DSP 21 in Figure 9) configured to access a single external memory in a single package (D-RAM 41 in Figure 9),

an access determination unit configured to determine, which each of the DSPs issues a read command or a write command at a same time, which one of the DSP is allowed to access the memory (MUX 114 and controller 104 receive signals from each DSP and Host 17, controlling which DSP is allowed to access the D-RAM, thus determining which DSP has access to the memory, see Figure 9 and Column 9 Lines 30-59);

a read/write control unit configured to control, when each of the DSPs issues the read command or the write command at the same time, the command of the allowed DSP (MUX 114 and controller 104 act as control means to receive signals from each DSP and Host 17, controlling which DSP is allowed to access the D-RAM, thus controlling read/writes, see Figure 9 and Column 9 Lines 30-59);

a first selector for outputting an address from the allowed DSP in response to a determination signal from the access determination means (signal C+D outputs the address from the allowed DSP, see Figure 9 and Multiplexer 114);

a second selector configured to output data from the allowed DSP in response to the determination signal (signal A+D outputs the data from the allowed DSP, see Figure 9 and Multiplexer 142, also Column 9 Lines 9-17), wherein;

each of the DSPs includes a control unit configured to acquire data from the external memory in response to the determination signal from the access determination

unit (each DSP can acquire data from the external memory in response to its allowed memory access, and thus has a control means to acquire data, DSP 2 through latch 126 and DSP 1 through latch 136, Column 9 Lines 4-9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have used the DSP system of Davis in the device of Kutaragi, because the shared memory of the signal processors in Davis's system allow for easy access between the processors without formal interruptions of the DSPs (Column 4 Lines 5-8 in Davis), thus increasing performance. So by combining the two devices, additional benefits are obtained.

**Regarding Claim 6**, Davis and Kutaragi teach the data processor according to Claim 5, wherein the read/write control unit does not access the external memory when each of the DSPs simultaneously issues a command (see Figure 5 of Davis, where the decode and form stages of the pipeline do not involve a memory access, and since DSP 1 and DSP 2 cannot access memory at the same time, when DSP 1 is reading or writing data, DSP 2 is executing a command but is not accessing the memory).

**Claim 3** is a broader version of Claim 5, and is rejected under similar rationale.

**Claim 4** is a broader version of Claim 6, and is rejected under similar rationale.

## **ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS**

### **Specification Objections**

Applicant's arguments/amendments with respect to the specification have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

**Claim Objections**

Applicant's arguments/amendments with respect to the claim objections of claims 1-6 have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

**Rejections - USC 112**

Applicant's arguments/amendments with respect to claims 4 and 6 have been considered and have overcome the Examiner's prior rejections and thus are withdrawn.

**ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

**Rejections - USC 102/103**

Applicant's arguments with respect to claims 1 and 2 that Kutaragi does not teach or suggest a DSP configured to use a selectable number of bus cycles in a unit of one data access has been considered but is not persuasive. Even though Kutaragi describes adjusting DSP and CPU memory accesses into equal intervals within a single machine cycle (Column 16 Lines 23-27), the number of bus cycles used between the DSP and CPU are selectable. Note particularly "the DSP 10 and the CPU 13 can share the single external RAM 14 in a time-division manner", Column 16 Lines 59-61, and that though the device of Kutaragi shows just one particular division of cycles for the DSP and the CPU, the various control signals (such as the change-over switch in Figure 12F) can be adjusted to select the number of bus cycles in a unit of one data access by adjusting how many cycles are used for the DSP and how many are used for the CPU.

Applicant's arguments with respect to claims 1 and 2 that Kutaragi does not teach a data word length accessed by a DSP at an external memory is variable has

been considered but is not persuasive. The adjustment of cycles described regarding the previous argument adjusts the amount of cycles the DSP has access to the memory, thus adjusting the length of the data word accessed based on the change-over switch.

Applicant's arguments regarding claims 3 and 5 that Davis does not teach an access determination unit configured to determine, when each of a plurality of DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access the memory has been considered but is not persuasive. Even though the processors 20 and 21 may be mutually exclusive, the access determination unit (corresponding to multiplexer 114) is configured to determine which one of the DSPs is allowed to access the memory based on the select input of the multiplexer.

## **CLOSING COMMENTS**

### **Conclusion**

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

#### **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

#### **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-6 have received a second action on the merits and are subject of a second action final.

#### **DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner  
Art Unit 2185

September 11, 2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185